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1. Title of the Invention: Method of Manufacturing Semiconductor Device

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SPECIFICATION

1. Title of the Invention

Method of Manufacturing Semiconductor Device

2. Scope of Claim for Patent

1) A method of manufacturing a semiconductor device comprising at least, (a) a step of forming a semiconductor layer mainly containing silicon on an insulating amorphous material, (b) a step of conducting crystal growth of the semiconductor layer with a heat treatment and so on, (c) a step of treating the semiconductor layer at a predetermined heat treatment temperature higher than that of the step (b).

2) A method of manufacturing the semiconductor device described in claim 1 characterized in that the heat treatment temperature in the above respective steps is 700 °C to 1200 °C.

3) A method of manufacturing the semiconductor device described in claim 1 or 2 comprising a step of forming a gate insulating film characterized in that a maximum temperature in the step of forming the gate insulating film is lower than the heat treatment temperature in the above step (c).

4) A method of manufacturing the semiconductor device described in claim 1, 2 or 3 characterized in that the heat treatment of the above step (c) is conducted through an excimer laser.

3. Detailed Description of the Invention

[Field of the Invention in Industry]

The present invention relates to a method of manufacturing a semiconductor device, particularly, relates to a manufacturing method for forming a semiconductor element on an insulating amorphous material.

[Prior Art]

Attempts are made to form sophisticated semiconductor elements on an insulating amorphous substrate of glass, quartz and the like, or on an insulating amorphous layer of SiO_2.

Recently, a large scale liquid crystal display panel having high resolution, a high speed contact type image sensor having high resolution and a three dimension IC and the like come to be needed. And a sophisticated semiconductor element on an insulating amorphous material above mentioned is hoped to be realized.

In case of forming a thin film transistor (TFT) on an insulating amorphous material, (1) TFT that an amorphous silicon formed with plasma CVD method or the like is used as an element material, (2) TFT that a polycrystal silicon formed with CVD method or the like is used as an element material, (3) TFT that a monocrystal silicon formed with melting recrystallization is used as an element material are examined.

However, of those TFTs, compared with electric field effect mobility in the case of using a monocrystal silicon as an element material, that of TFTs which an amorphous silicon and a polycrystal silicon are used as element materials is greatly lower (an amorphous silicon TFT < 1 cm^2 / V·sec, a polycrystal silicon TFT ~ 10 cm^2

/ V·sec). And a sophisticated TFT was difficult to be realized.

On the other hand, a melting recrystallization method with laser beam or the like is not yet enough completed technique. And in case that elements are necessary to be formed over a large area like in a liquid crystal display panel, there are big technical problems.

[Problem to be Solved by the Invention]

Then, as a simple and practical method to form a sophisticated semiconductor element on an insulated amorphous material, a method to grow a large polycrystal silicon in a solid phase state attracts attention and is researched. (Thin Solid Films 100 (1983) p.227, JJAP Vol. 25 No.2 (1986) p. L 121)

However, in the prior art, after a polycrystal silicon is formed with a CVD method, Si^+ is ion implanted to make the polycrystal silicon amorphous, and a heat treatment at about 600 °C is conducted for nearly 100 hours. Therefor, an expensive ion implantation device was needed and there was a defect that heat treatment hours were extensively long.

Then, the purpose of the invention is to provide a manufacturing method for forming a large polycrystal silicon having high crystallization in a more simple and practical method.

[Means to solve the Problem]

The manufacturing method of a semiconductor device in the present invention is characterized in that;

1) it comprises (a) a step of forming a semiconductor layer mainly containing silicon on an insulating amorphous material,

(b) a step of conducting crystal growth of the semiconductor layer with a heat treatment and so on,

(c) a step of treating the semiconductor layer at a predetermined heat treatment temperature higher than that of the step (b).

2) the heat treatment temperature in the above respective steps is 700 °C to 1200 °C.

3) the method comprises a step of forming a gate insulating film and the maximum temperature in a step of forming the gate insulating film is lower than a heat treatment temperature in the above step (c).

4) a heat treatment of the above step (c) is conducted with an excimer laser.

[Example]

Fig.1 is one example of a manufacturing process figure of the semiconductor device in the example of present invention. And, in Fig. 1, a thin film transistor is formed as a semiconductor element.

In Fig. 1, (a) is a step of forming a silicon layer 102 on an insulating amorphous substrate such as glass, quartz and so on, or on an insulating amorphous material 101 of an insulating amorphous material layer such as SiO_2. As an example of film formation condition, there is a LPCVD method at a temperature of 500 °C to 560 °C for forming a silicon film about 100 Å to 2000 Å in thickness. But, there is no limit to deposition methods.

(b) is a step of conducting crystal growth of the silicon layer 102 through heat treatment and the like. The optimum condition of heat treatment condition differs as to deposition methods of a silicon layer in the step (a). A polysilicon layer 103 is formed at a temperature of about 550 °C to 650 °C for about 2 to 30 hours in inactive gas atmosphere of nitrogen or Ar and the like.

(c) is a step of conducting heat treatment of the polysilicon layer 103 at a predetermined heat treatment temperature higher than that of that of the step (b). As a heat treatment temperature, there is an optimum value between 700 °C to 1200 °C. But in case of glass as a substrate, it cannot be exposed to the above high temperature. So it is important that the temperature of only the vicinity of the surface of the semiconductor is risen to the above temperature by irradiating short wave length light such as excimer and the like, and the irradiating intensity and the irradiating hours need to be optimized so that the temperature around the semiconductor layer and the substrate interface becomes under about 600 °C. As an example, the condition like the XeCl excimer laser (wave length 308 nm) is used and 1 to 10 pulse (1 pulse number + ns) is irradiated at the irradiating intensity about 0.1 to 1.0 J/cm^2 satisfies the above condition. When the temperature of a semiconductor layer and substrate surface is under about 600 °C during the laser irradiation, the condition melting a surface of a semiconductor layer is preferable because the crystallization of a semiconductor surface layer becomes better. Especially the surface layer is a region that an inversion layer is formed and crystallization improvement of a surface layer leads to an improvement of transistor characteristics.

(d) is a step of forming a gate insulating film 104. As a method for forming a gate insulating film, there is a thermal oxidation method at a high temperature 900 °C to 1200 °C (high temperature process). And there is a CVD method, a plasma CVD method, a light CVD method, a sputtering method and the like at a low temperature lower than about 650 °C (low temperature process). Of course, when glass is used as a substrate a low temperature process needs to be adopted.

(e) is a step of forming a semiconductor element. Fig. 1 (e) shows a case in which a TFT is formed as a semiconductor element. In the figure, 104 is a gate insulating film, 105 is a gate electrode, 106 is a source · drain region, 107 is an interlayer insulating film, 108 is a contact hole, 109 is a wiring. As an example of a TFT forming method, after forming a gate electrode, source · drain regions are formed by an ion implantation method, a thermal diffusion method, a plasma doping method, an ion shower doping method and the like. And an interlayer insulating film is formed through a CVD method, a sputtering method, a plasma CVD method and the like. Moreover, a contact hole is opened in the interlayer insulating film and wirings are formed. As a method of forming source · drain regions in case of using glass as a substrate, there is a method in which after impurities such as B, P and the like are implanted through an ion implantation method, those impurities are activated by a heat treatment at a low temperature about 600 °C for several to several ten hours. Also as other methods, an ion shower doping method, a plasma doping method and the like are effective.

In the present invention it is important that after a solid phase growth is made at a low temperature about 550 °C to 650 °C a heat treatment is conducted at a temperature higher than that. The reason is described below.

Crystallinity of the polycrystal silicon layer 103 that a crystal growth is conducted through a solid phase growth method in the step (b) is not necessarily high. Especially, conducting a solid phase growth of a silicon film (which is an amorphous silicon or a microcrystal silicon that a micro crystal region exists in the amorphous phase) formed through a LPCVD method at a comparatively low temperature about 500 °C to 560 °C, the crystallinity is about 50 to 70 % and low. Therefor, the process becomes important that crystallizes a not

crystallized region in the polycrystal silicon layer with a heat treatment at a higher temperature in the step (c) than the step (b). As a result, crystallinity can be risen to more than 99 %. Especially, when a gate insulating film is formed through the above low temperature process, conducting a heat treatment based on the present inveniton and promoting crystallinity are important because a high temperature heat treatment such as thermal oxidation is not made in the future process.

As a heat treatment method, in an annealing furnace and an atmosphere of nitrogen or an inactive gas such as Ar, for example, there are heat treatment methods for about an hour at 850 °C and 10 to 20 minutes at 1000 °C. In addition to that, there are methods of lamp annealing using a halogen lamp, arc lamp, infrared lamp, xenon lamp, mercury lamp and the like. And there are methods of laser annealing using an excimer laser, Ar laser, He-Ne laser and the like. Among them the laser annealing using an excimer laser can be used when a cheap glass substrate is used because it can heat only the around surface of a semiconductor layer. In such a case the crystallinity of at least from the surface of the semiconductor layer to several hundred Å can be made more than 99 %. As a result, if a gate insulating film is formed through a low temperature process, and source · drain regions are formed through a low temperature process less than about 600 °C (for instance, the method that activation is conducted through a heat treatment about 600 °C for several to several ten hours after implanting impurities such as B, P and the like by an ion implantation method.), a sophisticated semiconductor element can be formed on a glass substrate and the effect is quite large. Comparing the case that laser annealing is conducted after a solid phase growth at about 550 °C to 650 °C with the case that laser annealing of the as-depo sited film without a solid phase growth, crystal grain sizes of the films with the solid phase growth is large (more than 1 μm) and crystallinity is high (in the case of only the laser annealing, the crystallinity of the semiconductor layer around a substrate is especially bad).

Moreover, an important correlation is discovered between the film deposition temperature through a LPCVD method and the existence of the heat treatment in the step (c). That is, comparing a silicon layer formed through the LPCVD method at a high temperature (for example about 580 °C to 610 °C) and a silicon layer at a low temperature (for example about 500 °C to 550 °C), if there was no heat treatment in the step (c), though a silicon layer formed at the low temperature was large in crystal grain size, crystallinity was low and the electric field effect mobility was small. However, if the heat treatment was conducted in the step (c), crystal grain size and crystallinity and electric field effect mobility of TFT of the silicon layer formed at a low temperature was large. And this was a value that could not be obtained from the film formed at a high temperature about 580 °C to 610 °C through the LPCVD method.

The reason is assumed as described below. (1) A film formed at a low temperature is an amorphous silicon or a microcrystal silicon in which a microcrystal region exists in the amorphous phase. Therefore, compared with a film formed at a high temperature, generation density of polycrystal nuclei at a solid phase growth is low and a large size polycrystal silicon can be formed with a sold phase growth. (2) However, concerning about a film formed at a low temperature, the portion of amorphous phase after a solid phase growth is large and a high temperature heat treatment seems to be necessary to raise crystallinity. Therefore, the present invention is effective

not only for a film formed through the CVD method, but for the cases where an amorphous silicon or a microcrystal silicon are formed through an evaporation method, a plasma CVD method, an EB evaporation method, a MBE method, a sputtering method, a CVD method. And the invention is also effective for the case where after a microcrystal silicon or a polycrystal silicon is formed through a plasma CVD method, a CVD method, an evaporation method, an EB evaporation method, a MBE method, a sputtering method and the like, elements such as Si, Ar, B, P, He, Ne, Kr, H and the like are ion implanted to make a whole or a portion of the microcrystal silicon or the polycrystal silicon in an amorphous state. Particularly, the present invention is more effective to an as-deposited film having a higher proportion of an amorphous phase and a lower nucleous density of polycrystal a film that the amorphous phase portion of the as-depo film is high and the generation density of polycrystal (namely, a large size polycrystal silicon is easy to form through a solid phase growth).

The electric field effect mobility of a polycrystal silicon TFT (N channel) using the manufacturing method of a semiconductor device based on the present invention and formed through a low temperature process is about 150 to 200 m^2 / V·sec, and the same character as the TFT formed through a thermal oxidation method is obtained.

Though the present invention is the most effective in the above low temperature process, it is also effective in a high temperature process. That is to say, when a polycrystal silicon having large non-crystallized regions is oxidized thermally, the non-crystallized regions having a higher oxidation speed than crystallized regions are oxidized first. As a result, an oxidation film is formed along a crystal grain boundary and the mobility is decreased. However, using an annealing method of the present invention , since crystallinity before thermal oxidation is increased sufficiently and the oxidation along the crystal grain boundary is suppressed, the effect is quite large.

Moreover, providing the above TFT manufacturing process with a process exposing the semiconductor element to a plasma atmosphere of a gas including at least hydrogen gas or ammonium gas and hydrogenating the above TFT, defect density existing in a crystal grain boundary can be decreased and the above electric field effect mobility can be improved.

And the method of doping impurities into the channel region and controlling Vth (threshold voltage) is also quite effective. In case of the polysilicon TFT formed through a solid phase growth method, Vth of the N channel transistor shifts to the depression direction and the P channel transistor shifts to the enhancement direction. And, the tendency becomes more remarkable in the case of hydrogenating the TFT as described above. Then, doping impurities about 10^{15} to 10^{19} / cm^3 into the channel region, a shift of Vth can be restrained. For example, there is a method in the Fig 1, before forming the gate electrode, we implant impurities such as B (boron) and so on at a dose of about 10^{11} to 10^{12} /cm^2 through ion implantation method and the like. Particularly, with the dose amount as said before, Vth can be controlled so as to minimize the off current of both a P channel transistor and a N channel transistor. Therefore, in case of forming a TFT element of the CMOS type, channel doping of the entire surface in the same process can be performed without selective channel doping of Pch and Nch.

And the present invention can be applied not only to the TFT shown in an example of Fig.1, but also to all insulated gate type semiconductor elements. In addition to that, the invention is extremely effective in the case of

forming semiconductor elements using a polycrystal semiconductor as an element material, such as bipolar transistors, elctrostatic induction type transistors, photoelectric conversion elements such as solar cells and light sensor.

[Effect of the Invention]

As mentioned above, according to the present invention, in a more simple manufacturing process, a large size polycrystal silicon film having high crystallinity can be formed. As a result, a sophisticated semiconductor element can be formed on insulated amorphous material and it becomes easy to form a big liquid crystal display panel having high resolution, a high speed contact type image sensor having high resolution, a three dimensions IC and the like.

And the present invention can be applied not only to the TFT shown in an example of Fig.1, but also to all insulated gate type semiconductor elements. In addition to that, the invention is extremely effective to form photoelectric conversion elements such as bipolar transistors, electrostatic induction type transistors, solar cells and light sensor using a polycrystal semiconductor as an element material.

4. Brief Explanation of the Drawings

Fig. 1 (a) to (e) are manufacturing process figures of a semiconductor device in the example of the present invention.

101--- insulated amorphous material
102--- silicon layer
103--- polycrystal silicon layer
104--- gate insulating film
105--- gate electrode
106--- source・drain region
107--- interlayer insulating film
108--- contact hole
109--- wiring

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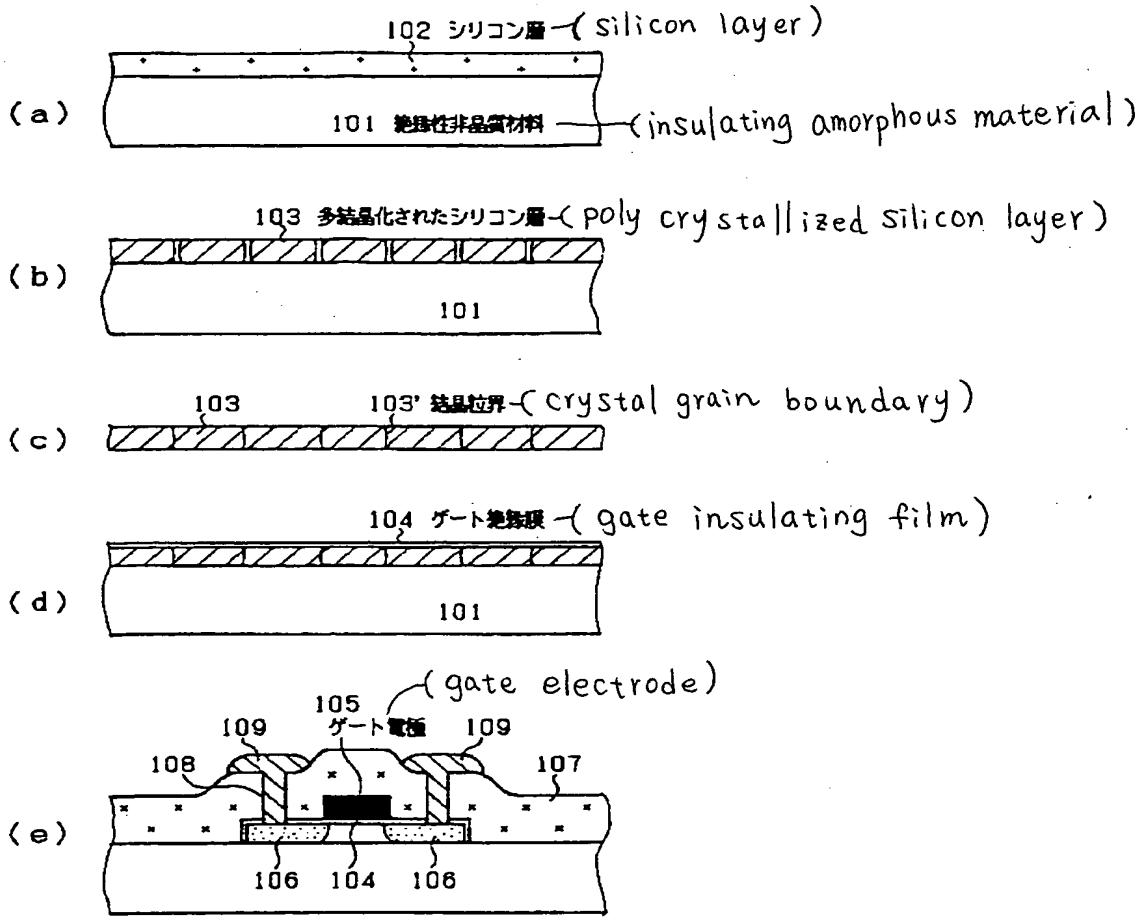
102 シリコン層 (silicon layer)
(a)
101 絶縁性非晶質材料 (insulating amorphous material)
103 多結晶化されたシリコン層 (poly crystallized silicon layer)
(b)
101
103
103' 結晶粒界 (crystal grain boundary)
(c)
104 ゲート絶縁膜 (gate insulating film)
(d)
101
(gate electrode)
105
ゲート電極
109
109
108
107
(e)
106
104
106

第 1 図